**ECE 429 Lab 5**

**Hierarchical Design and Formal Verification**

**David Cho**

**A20384999**

**02/27/2020**

**Introduction**

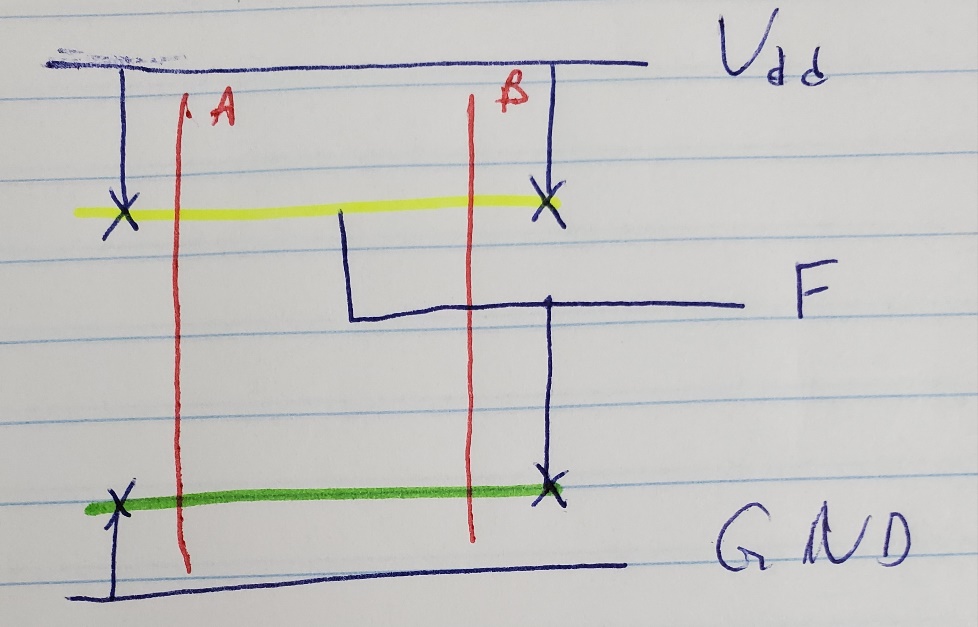
The objective of this lab is to be introduced to hierarchical design, as well as formal verification techniques that are essential for complex circuit designs. This will be accomplished by building and testing a 2-input AND gate.

**Theory/Pre-Lab**

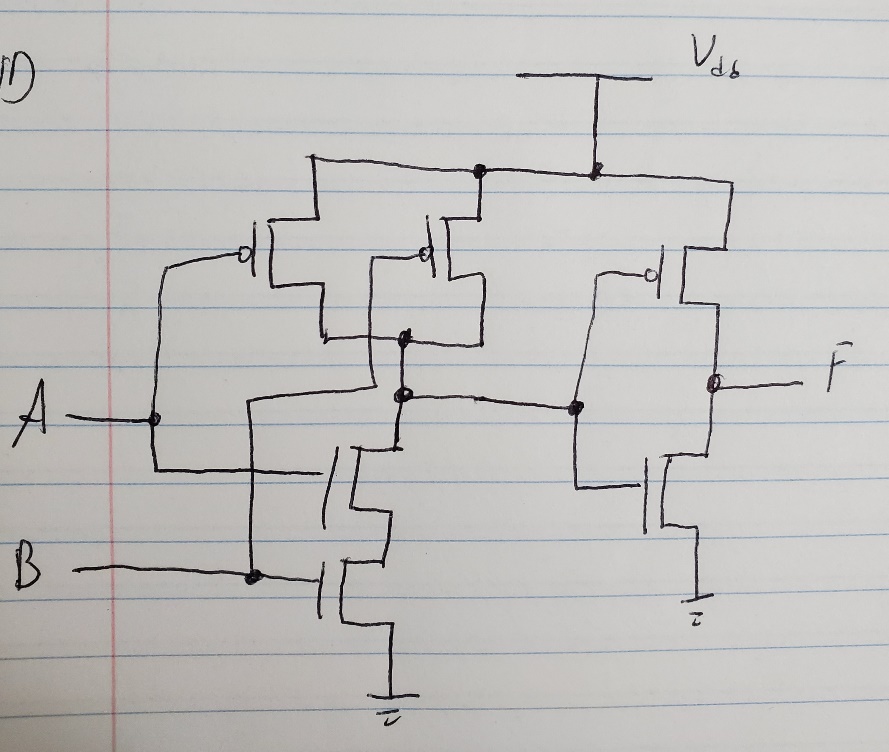
Chip fabrication is a very expensive process, so it is now a must to verify that a chip works correctly before sending the design for takeout. Functional verification validates the logic functionality of the design but becomes too time consuming with larger amounts of inputs, since every possible pattern would have to be simulated and tested. Formal verification techniques are proposed to cut down on testing times and provide a proof of correctness. In this experiment, equivalence checking will be utilized. Equivalence checking proves or disproves that two chosen designs provide the same functionality. The Formality ESP tool will be used to properly test the design.

Before beginning the lab, a stick diagram for a 2-input NAND gate was sketched, followed by a sketch of a 2-input AND gate at the transistor level. The AND gate was designed using both a NAND gate and an inverter.

**Figure 1: 2-input NAND Gate Stick Diagram**

****

**Figure 2: AND Gate Design**



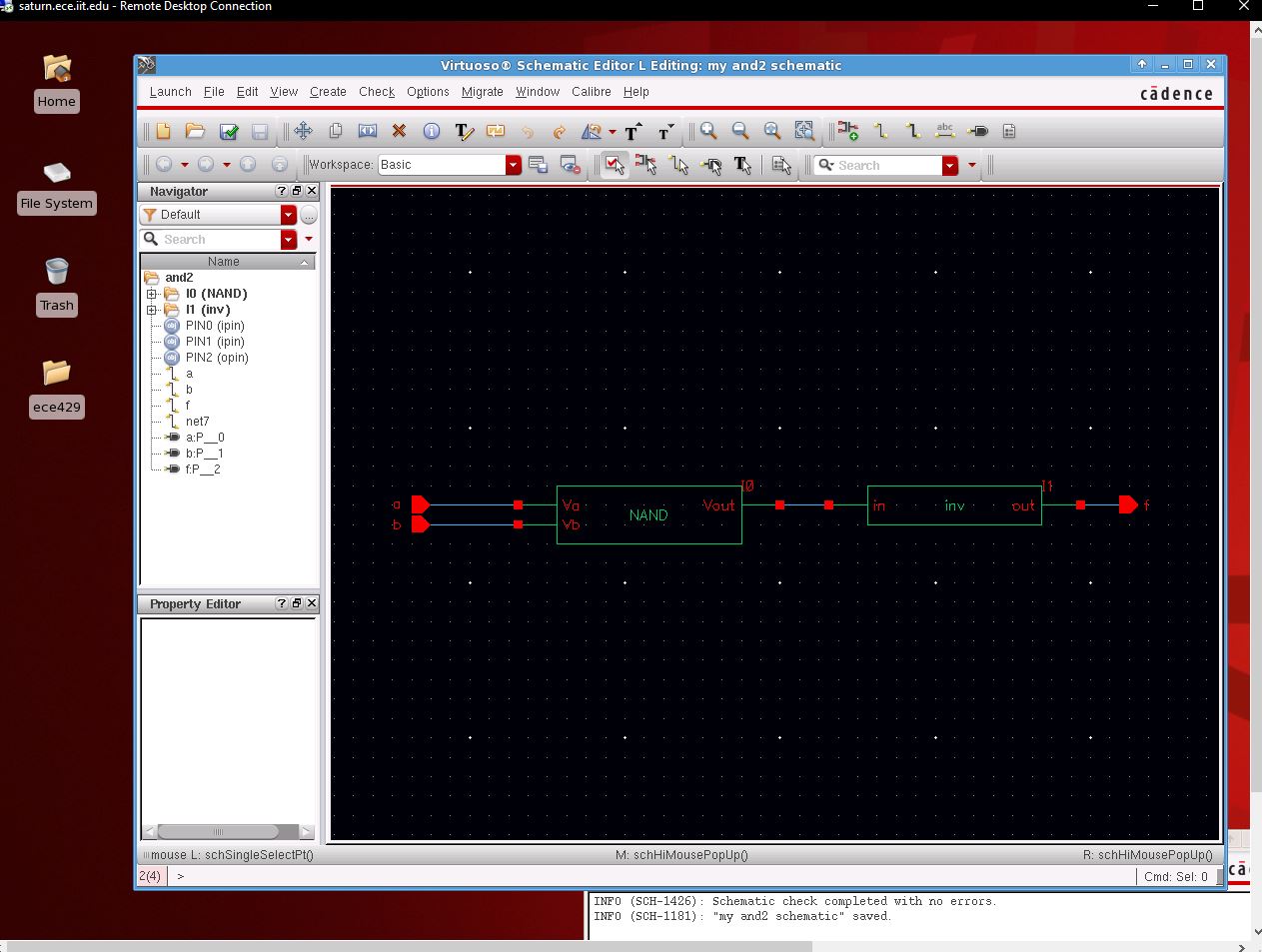
The AND gate design utilizes a NAND gate and an inverter. The left four transistors signify the NAND design, and the right two transistors signify the inverter.

In addition to the two sketches, the Tutorial III provided in the lab manual was read as part of the pre-lab.

**Implementation**

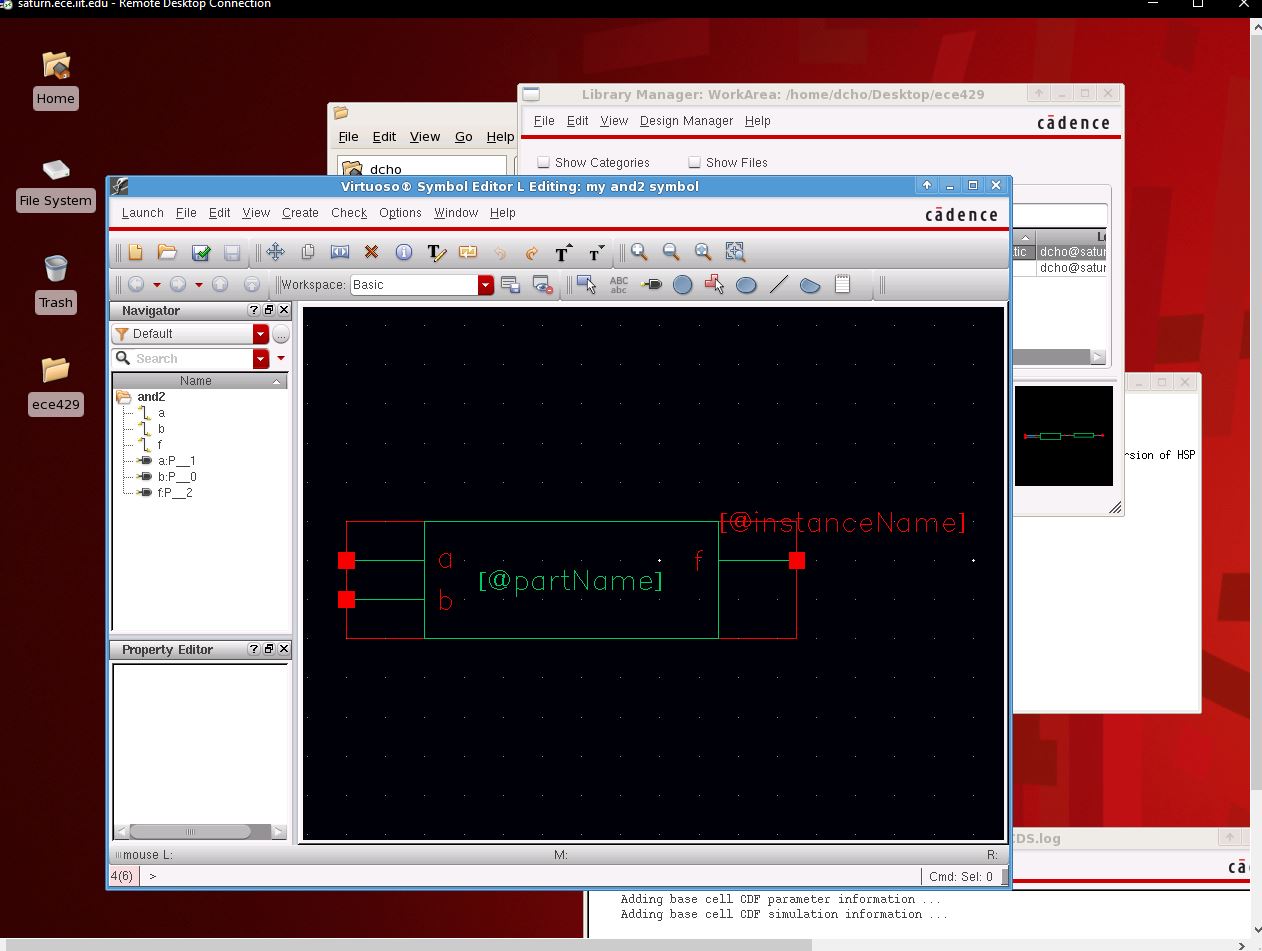
By utilizing the inverter and NAND symbols from previous labs, the schematic of the 2-input AND gate was created.

**Figure 3: AND Gate Schematic**

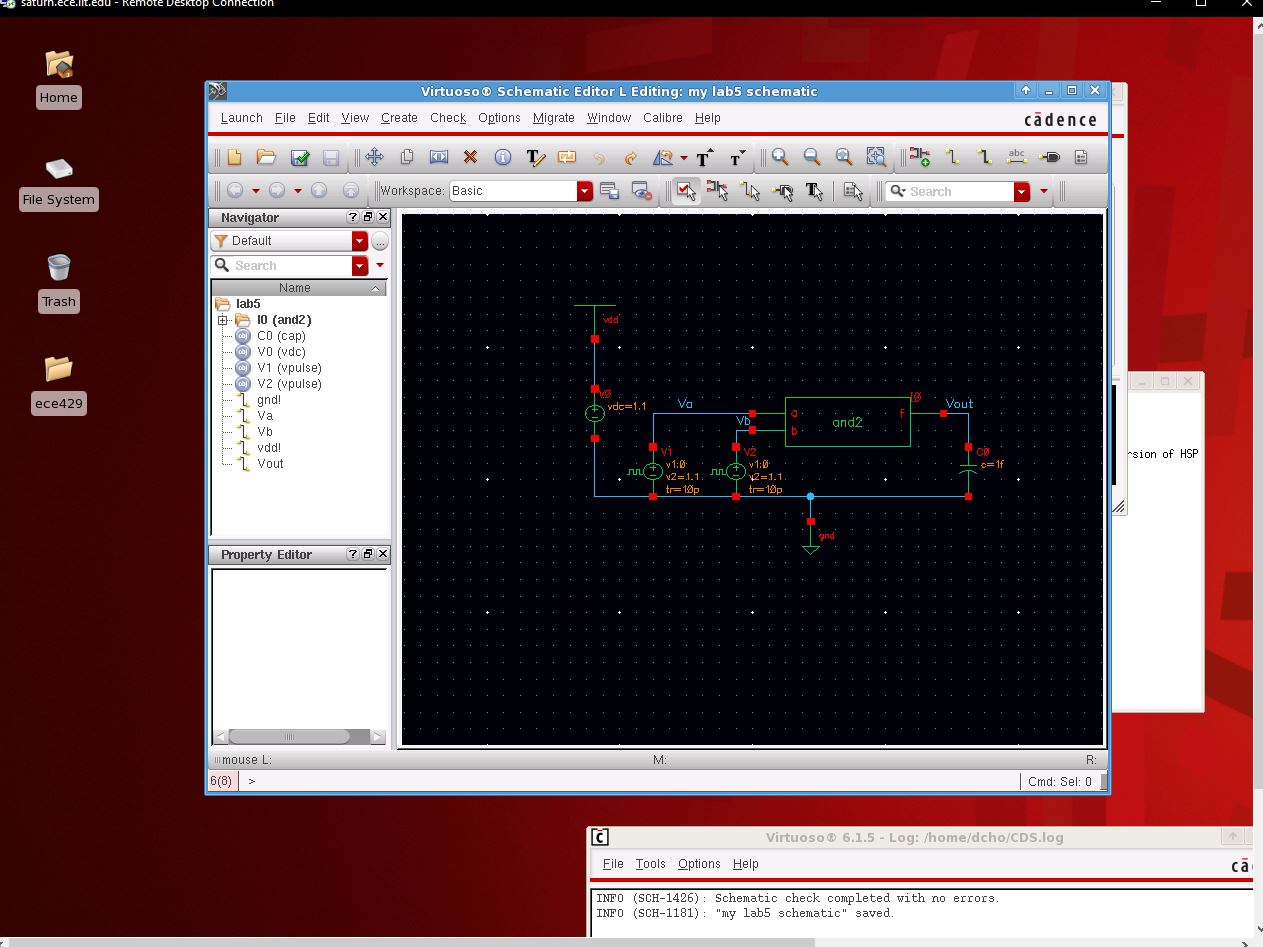


The symbol on the left is the NAND symbol, with its output going into the input of the inverter symbol. From that schematic, the AND gate symbol was created and utilized in a test circuit.

**Figure 4: AND Gate Symbol**

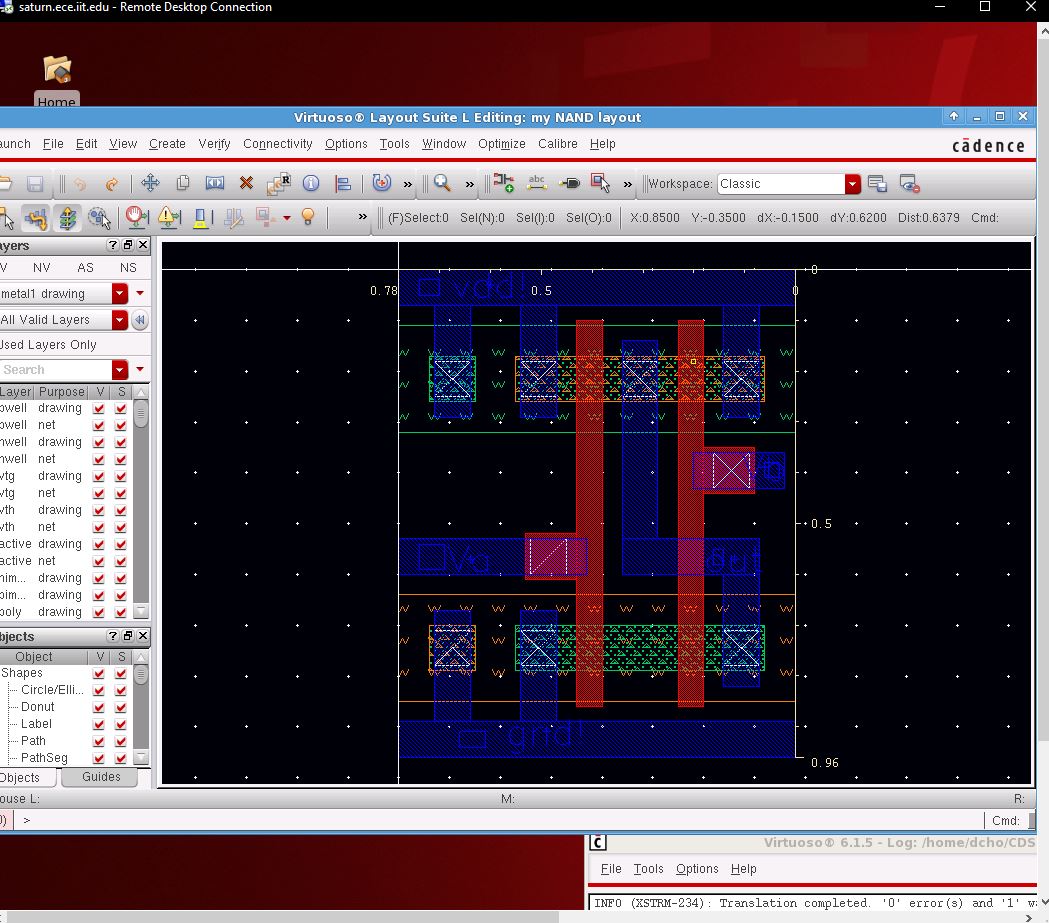
****

**Figure 5: AND Gate Test Circuit**

****

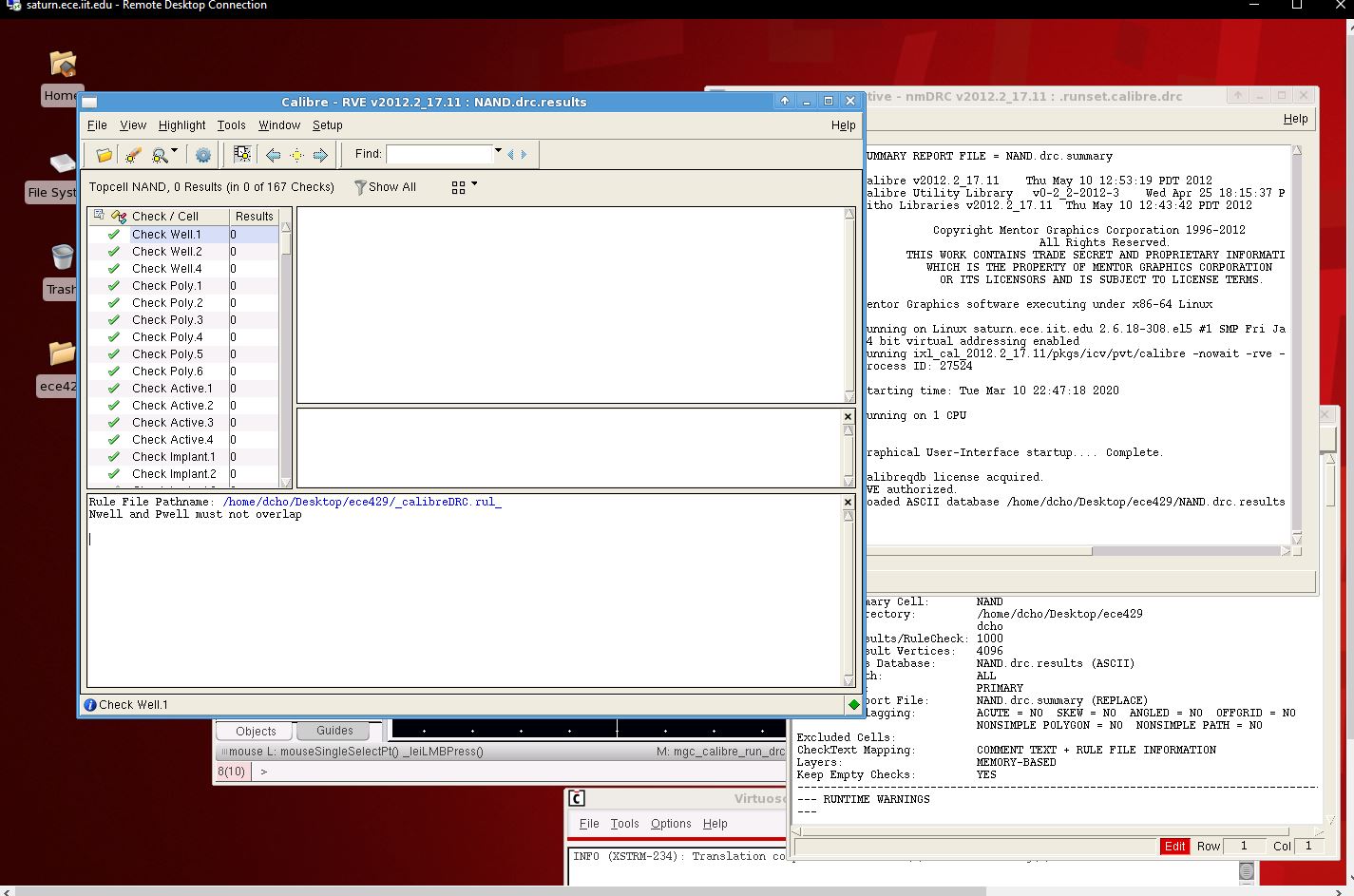
Using the sketch of the 2-input NAND gate stick diagram, the layout was created in Virtuoso.

**Figure 6: NAND Layout**

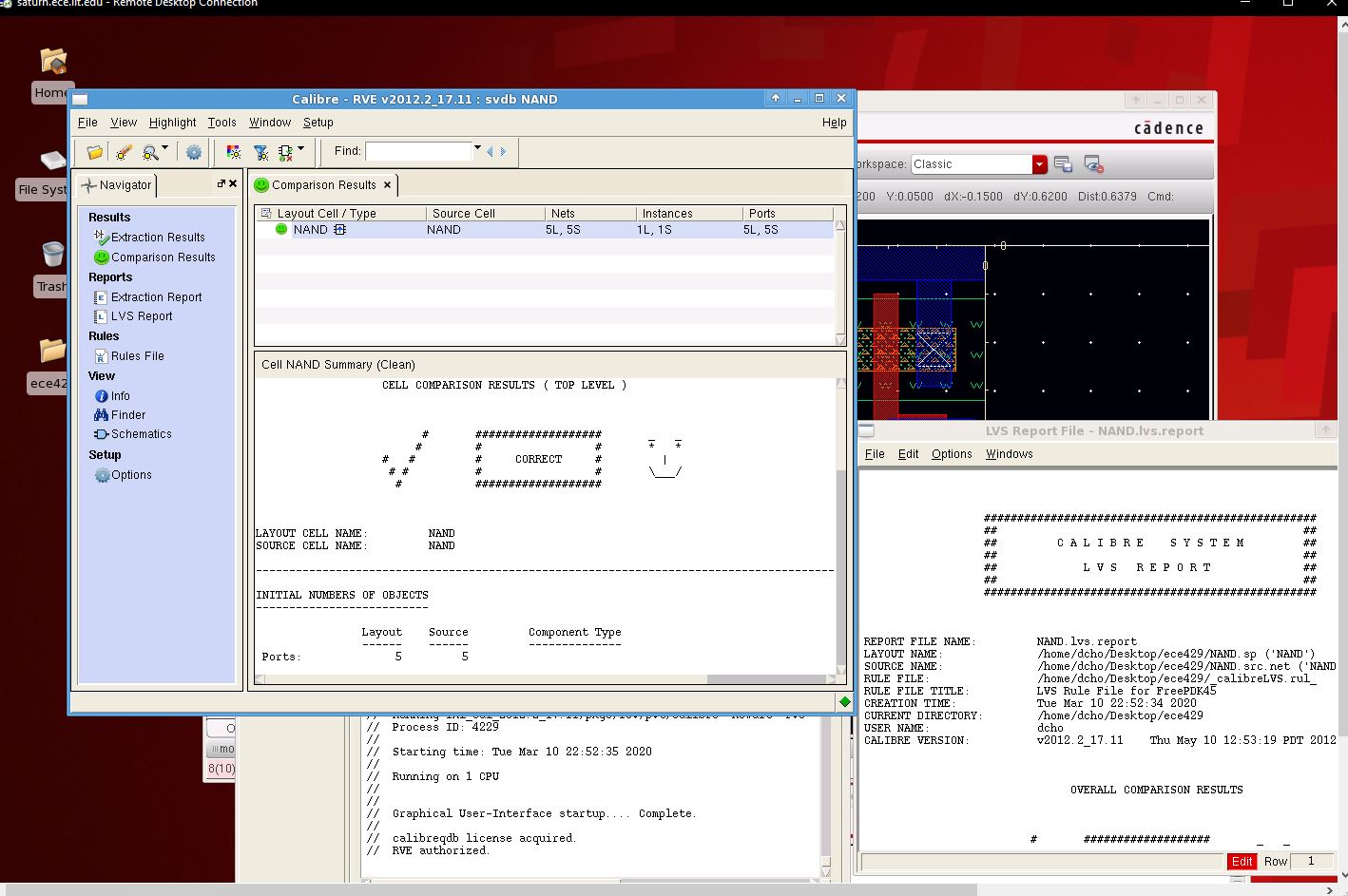
****

For rule and layout functionality checking, DRC and LVS were ran.

**Figure 7: NAND Layout DRC**

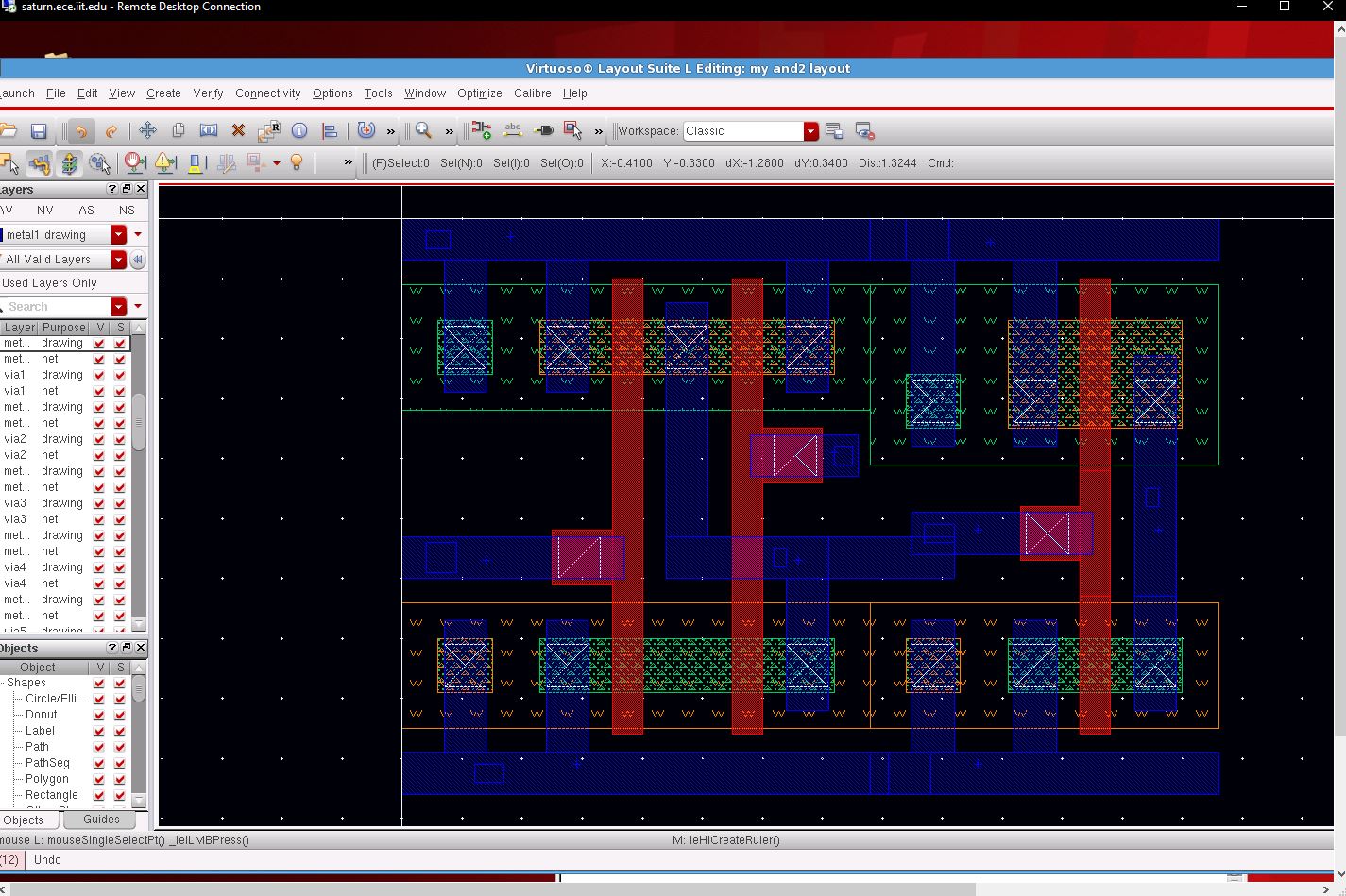
****

**Figure 8: NAND Layout LVS**

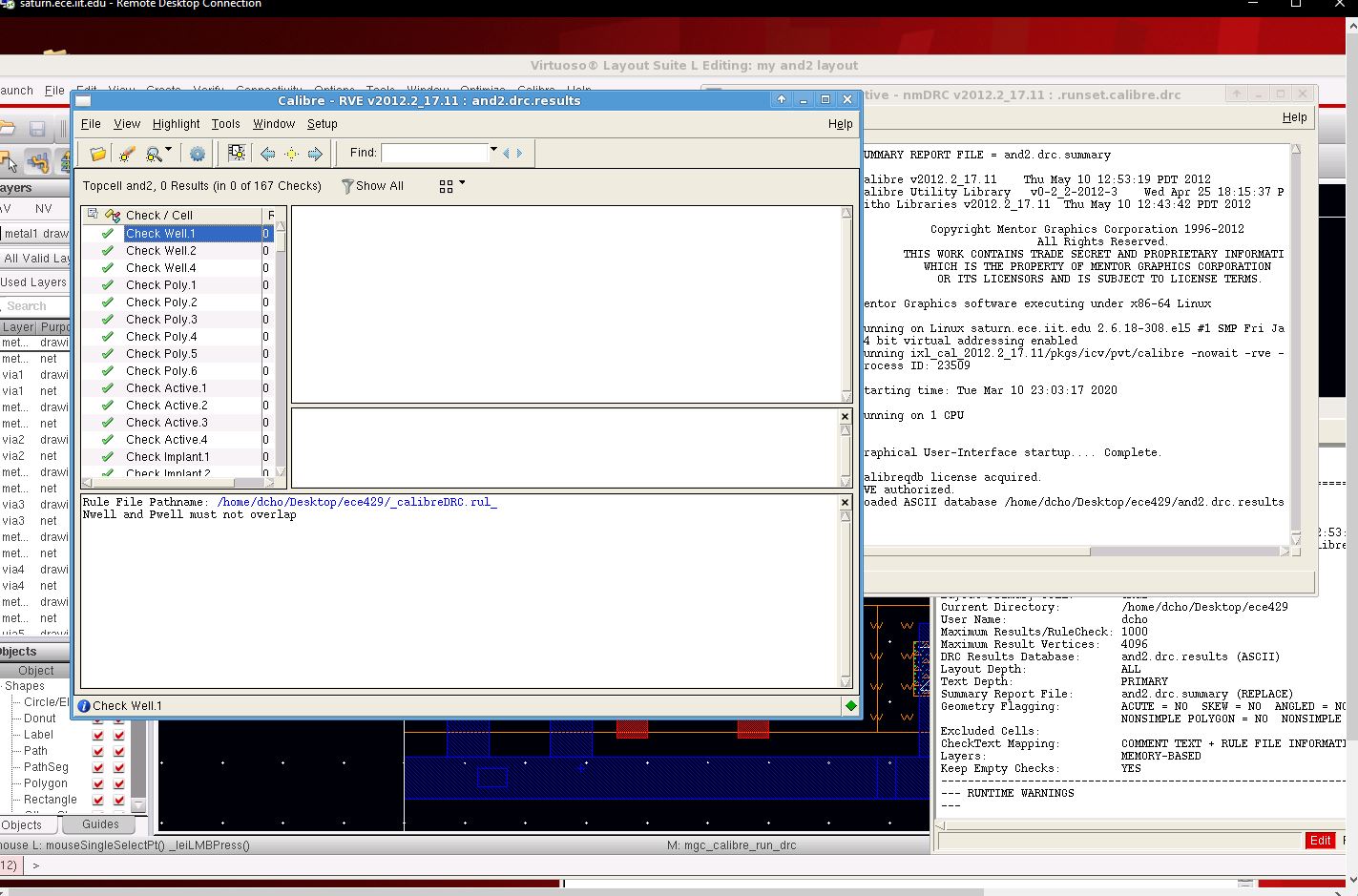
****

Once the NAND layout is created and verified, it is connected to the inverter layout to form the AND gate layout. The completed layout is checked using DRC and LVS.

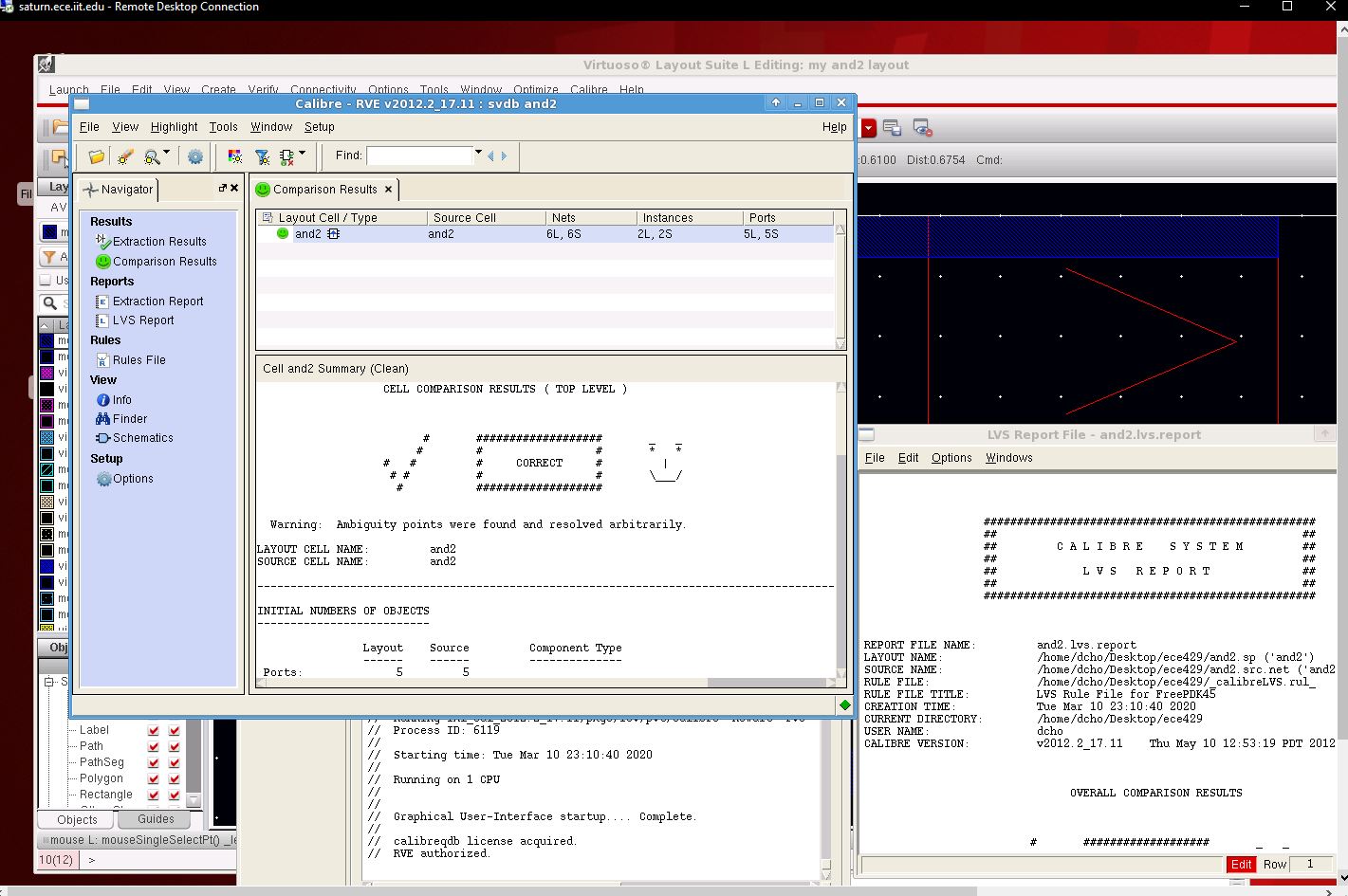
**Figure 9: AND Layout**

****

**Figure 10: AND Layout DRC**

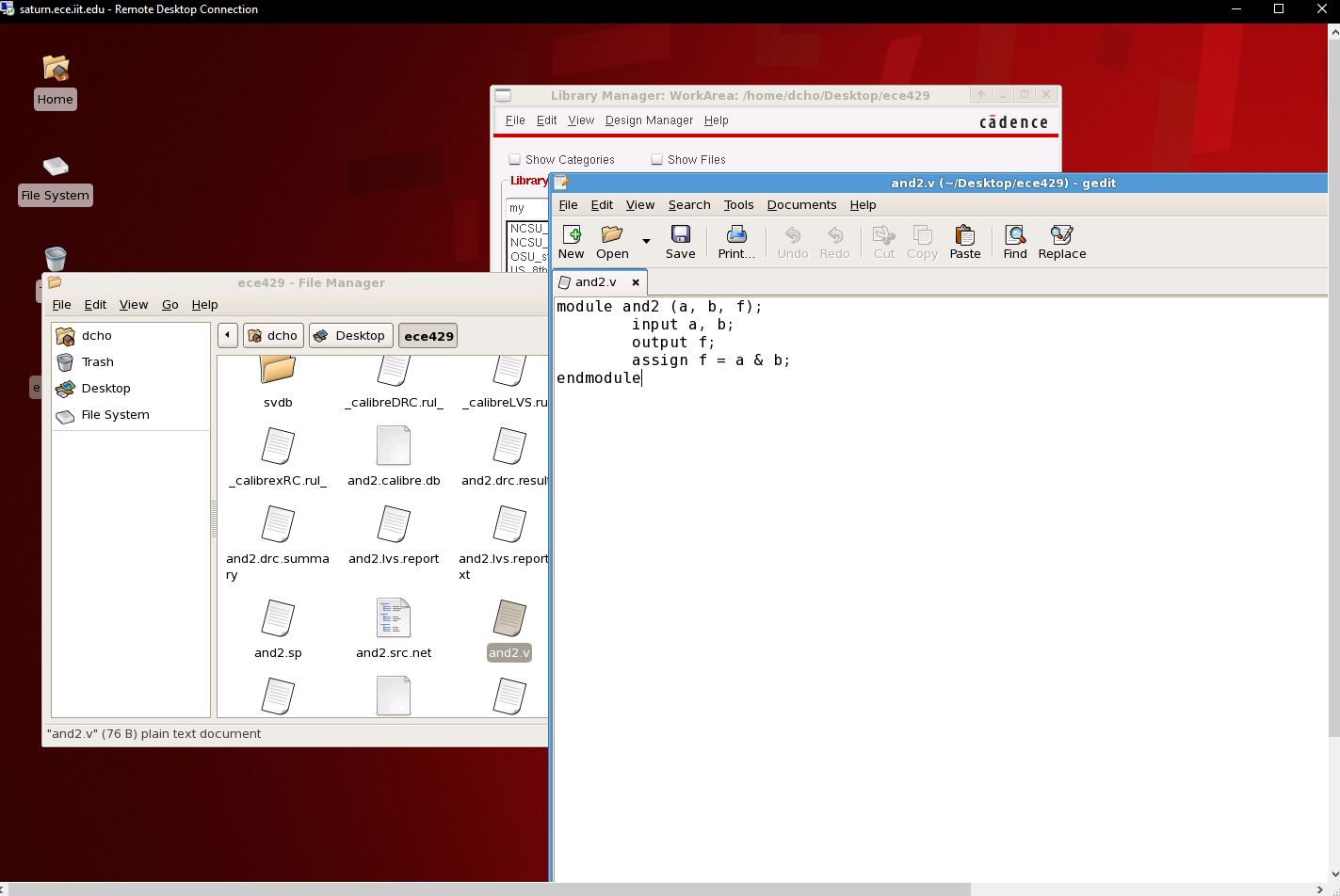
****

**Figure 11: AND Layout LVS**

****

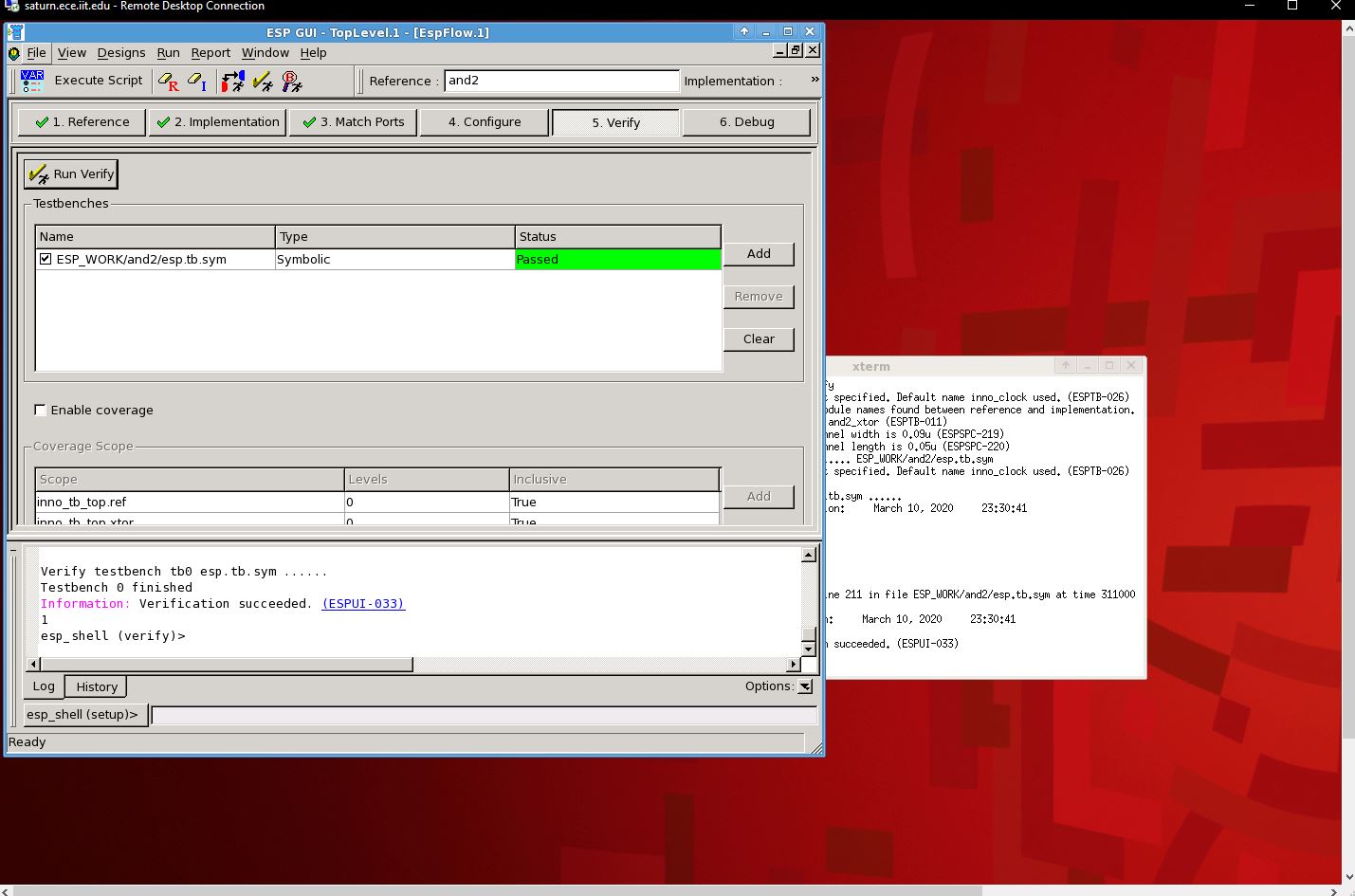
After the AND Layout is complete, it was time to use equivalence checking to verify the validity of the layout. First, a Verilog module of the AND gate was created.

**Figure 12: AND2 Verilog File**

****

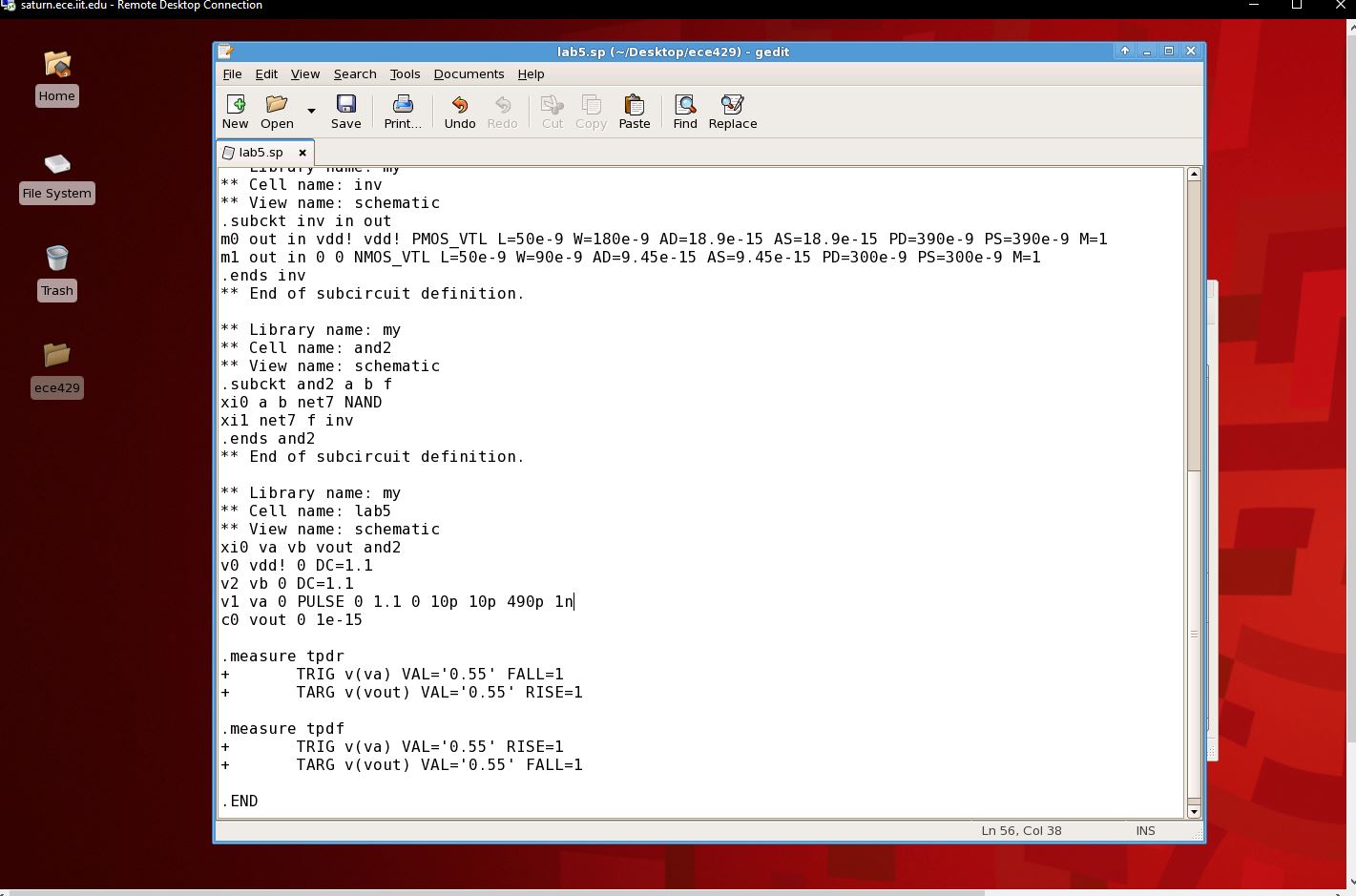
Using Formality ESP, the source file from the layout LVS was compared to the Verilog file. The test case was passed.

**Figure 13: ESP Result**

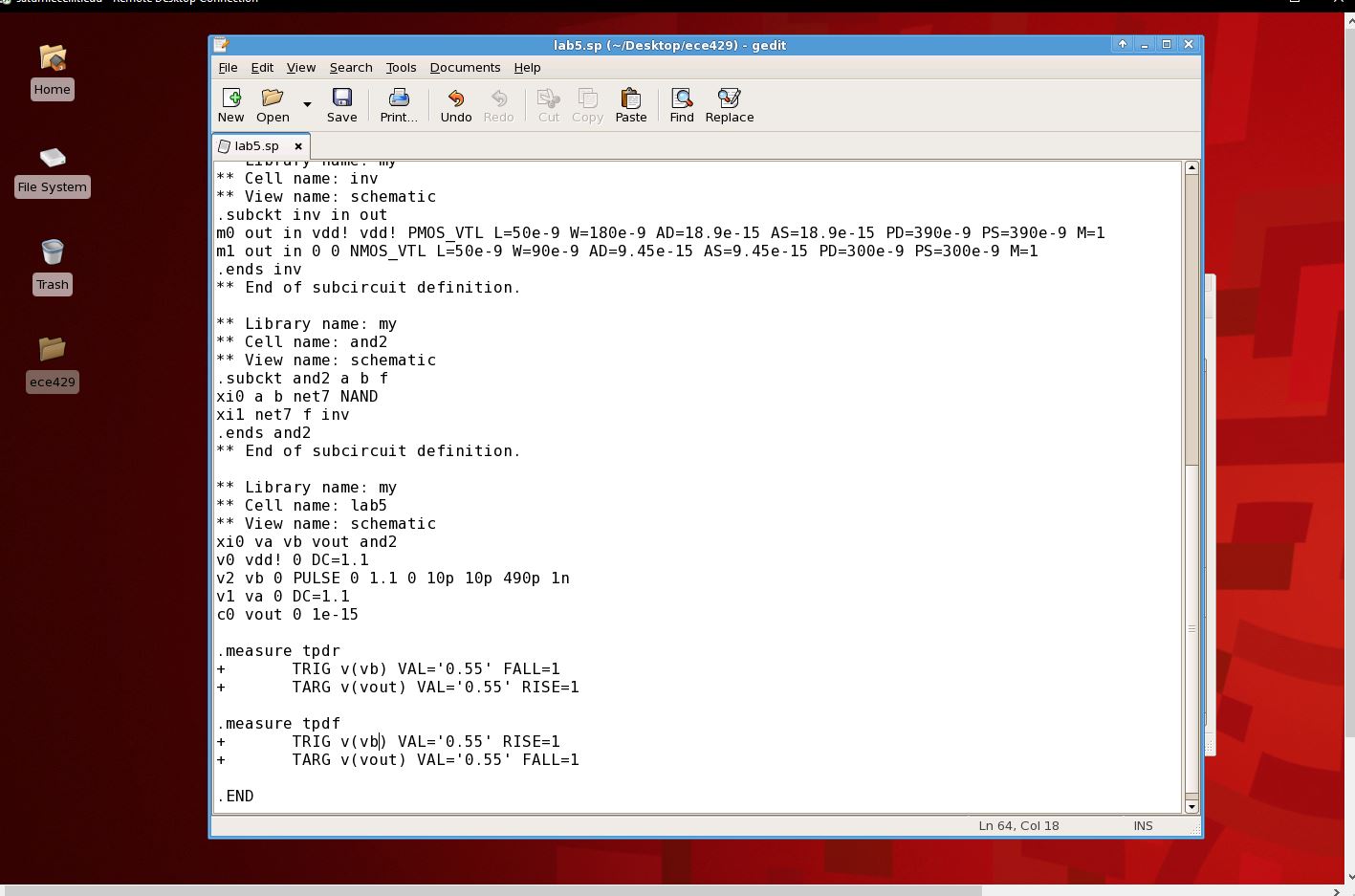
****

Just as in lab 4, three different excitation settings are simulated, with their delays measured. The netlists and measured delays are seen below.

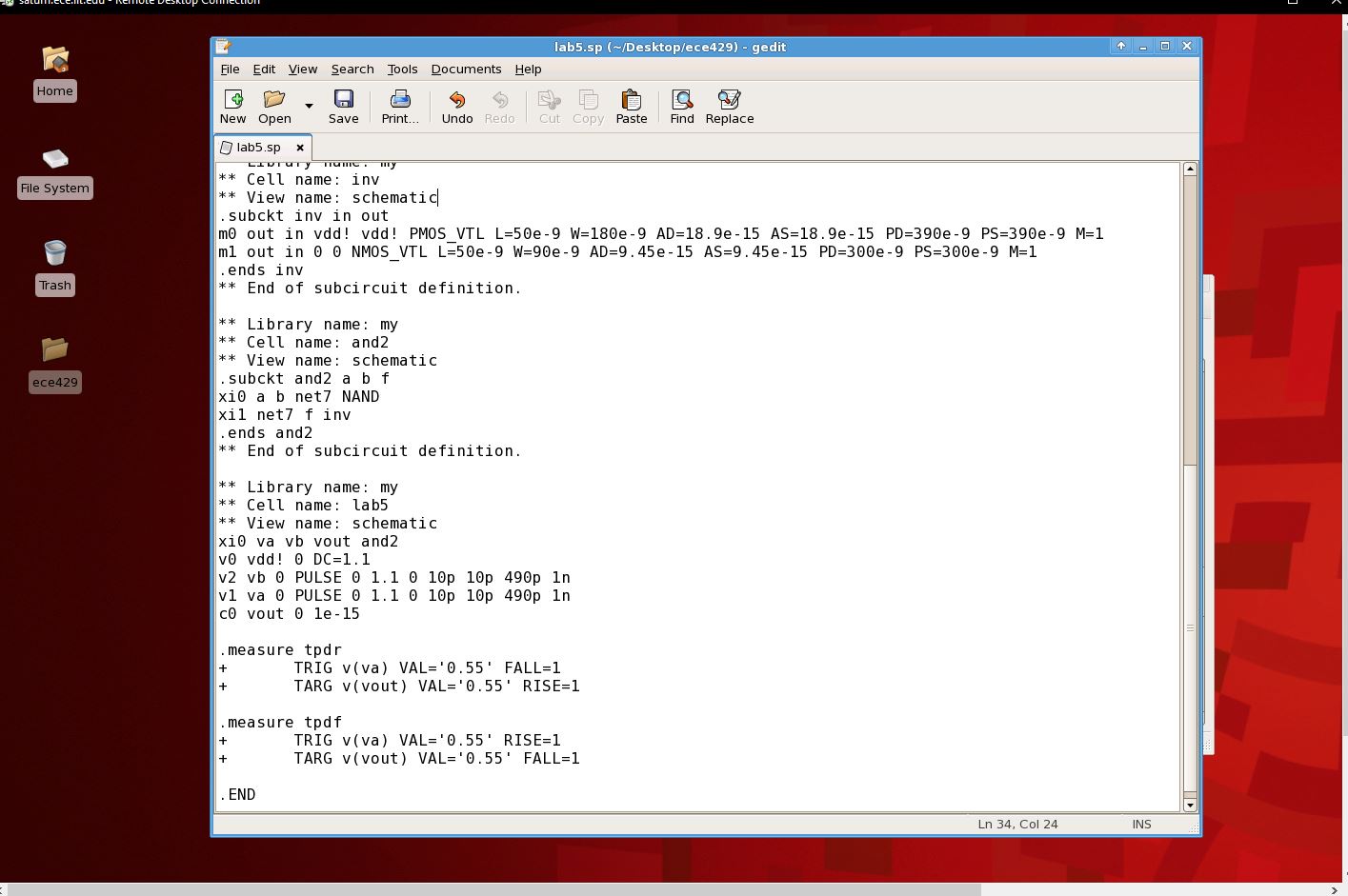
**Figure 14: 01🡪11 Netlist**

****

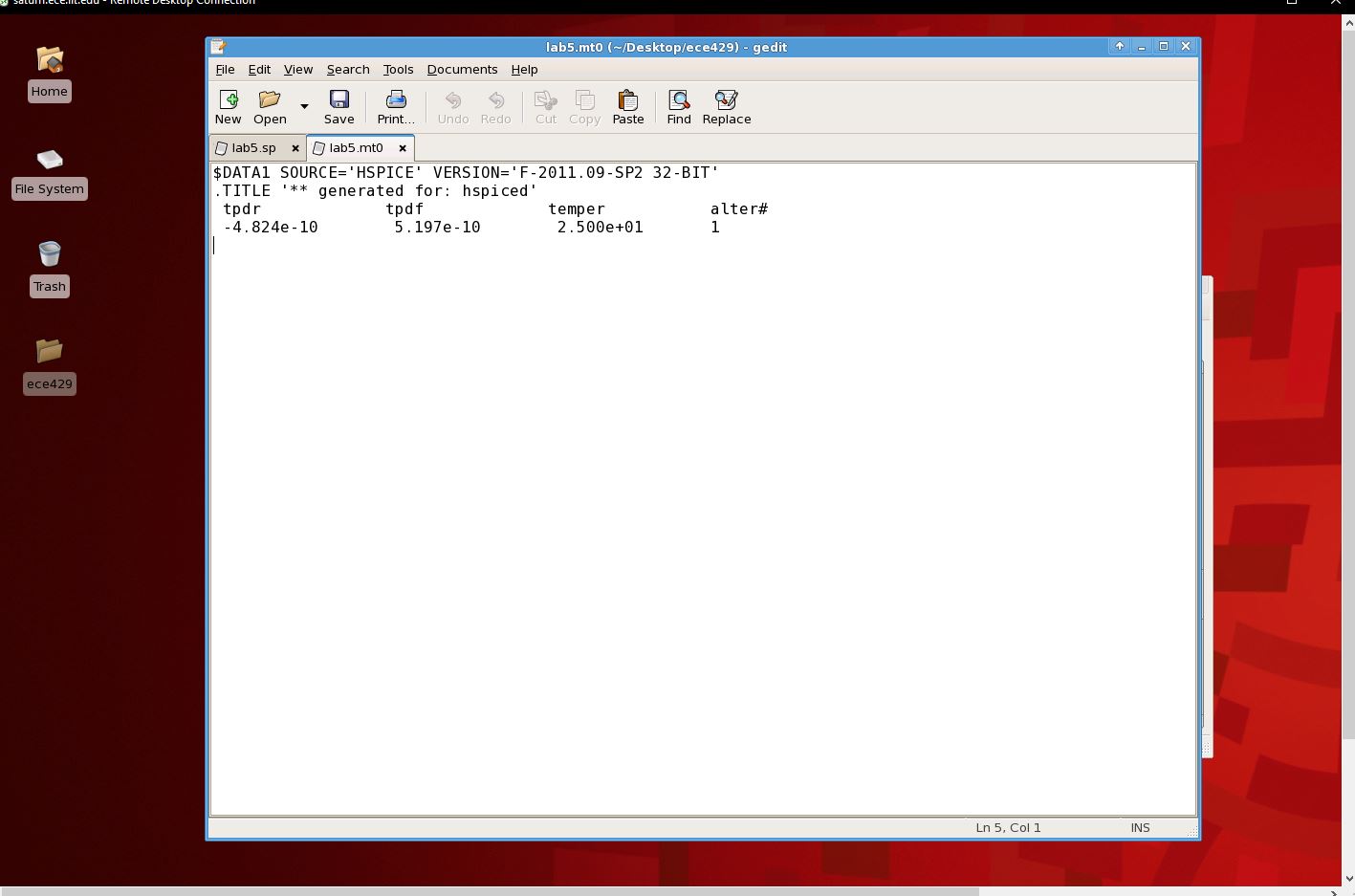
**Figure 15: 10🡪11 Netlist**

****

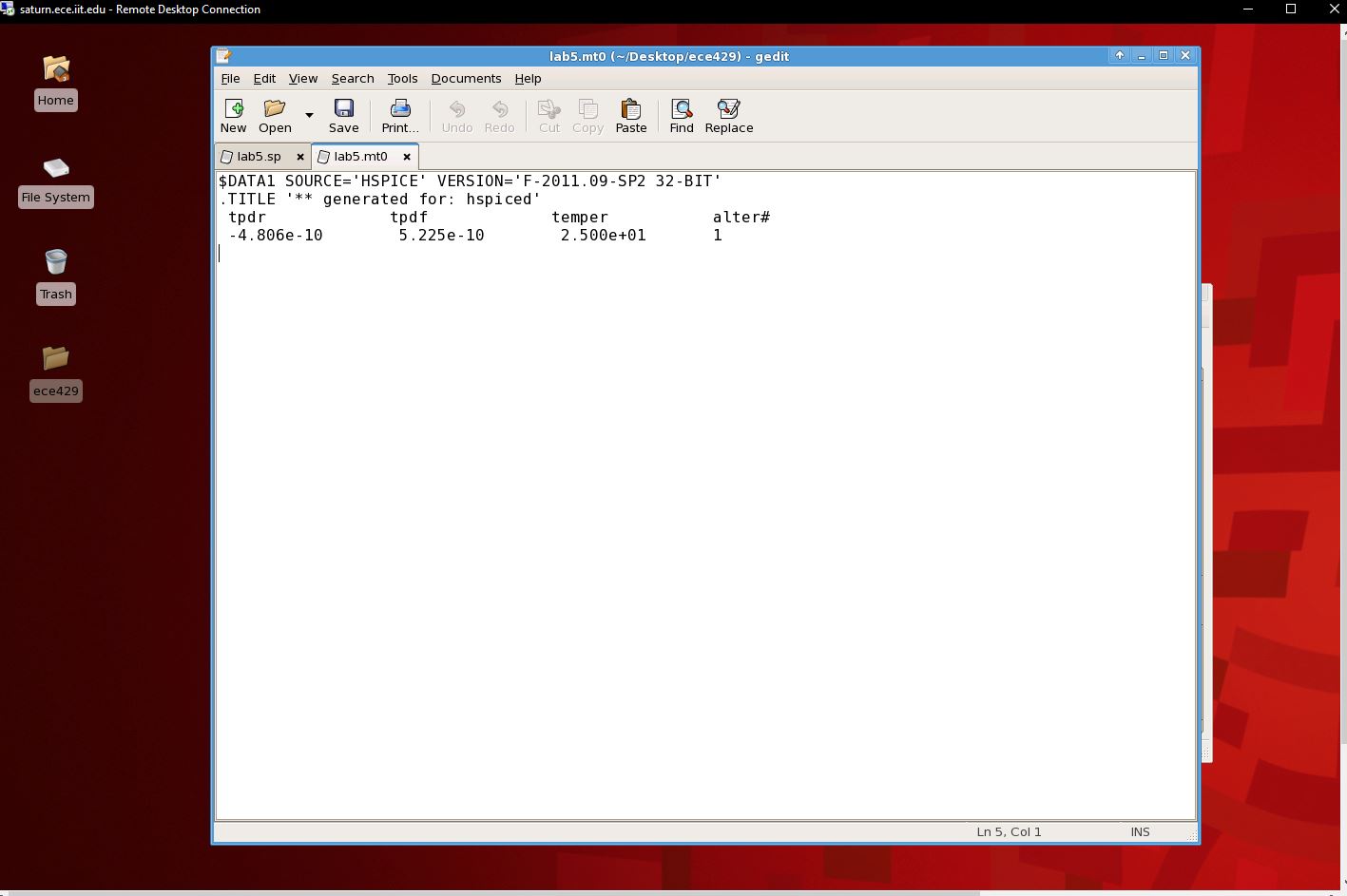
**Figure 16: 00🡪11 Netlist**

****

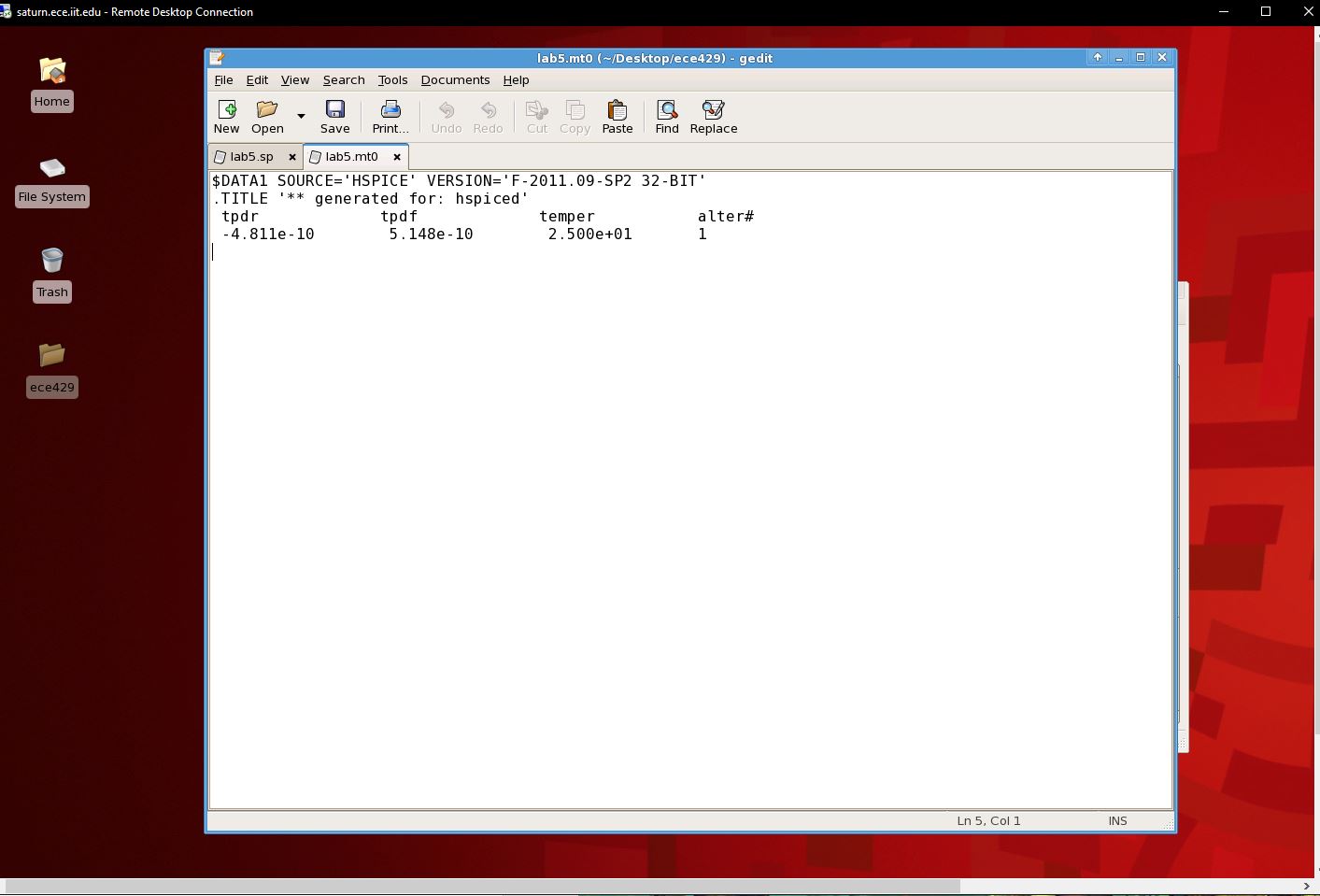
**Figure 17: 01🡪11 .mt0**

****

**Figure 18: 10🡪11 .mt0**

****

**Figure 19: 00🡪11 .mt0**

****

From the measurement file, the following delay table can be made.

|  |  |  |  |
| --- | --- | --- | --- |
| W: 90nm  L: 50nm  C: 1fF | **Input Transitions** | | |
| **01🡪11** | **10🡪11** | **00🡪11** |
| TPDR | 4.824e-10 | 4.806e-10 | 4.811e-10 |
| TPDF | 5.197e-10 | 5.225e-10 | 5.148e-10 |

**Deliverable Questions**

1. Instead of using an inverter with a NAND gate, the output of a NAND gate could be connected to another NAND gate (which could then act as an inverter) to form an AND gate. The method from the lab is far more preferable since it uses less transistors and takes less time to build. Utilizing another NAND gate is redundant.
2. The input transitions leading to the propagation delays do match my expectations. I expected they would be longer because the design is more complicated and layered.
3. From the measurements of the propagation delays, the delay from the AND gate seems to be about the sum between the lab 2 inverter and the lab 4 NAND gate.
4. A schematic is a visual representation of a layout, while a Verilog model represents the circuit with code.

**Conclusion**

In conclusion, this lab was successful. The 2-input AND gate was successfully created by utilizing the previous layout designs. The simulations also successfully ran and mostly gave the expected results. The functionality matched the expected functionality, and a Verilog equivalence check was passed.